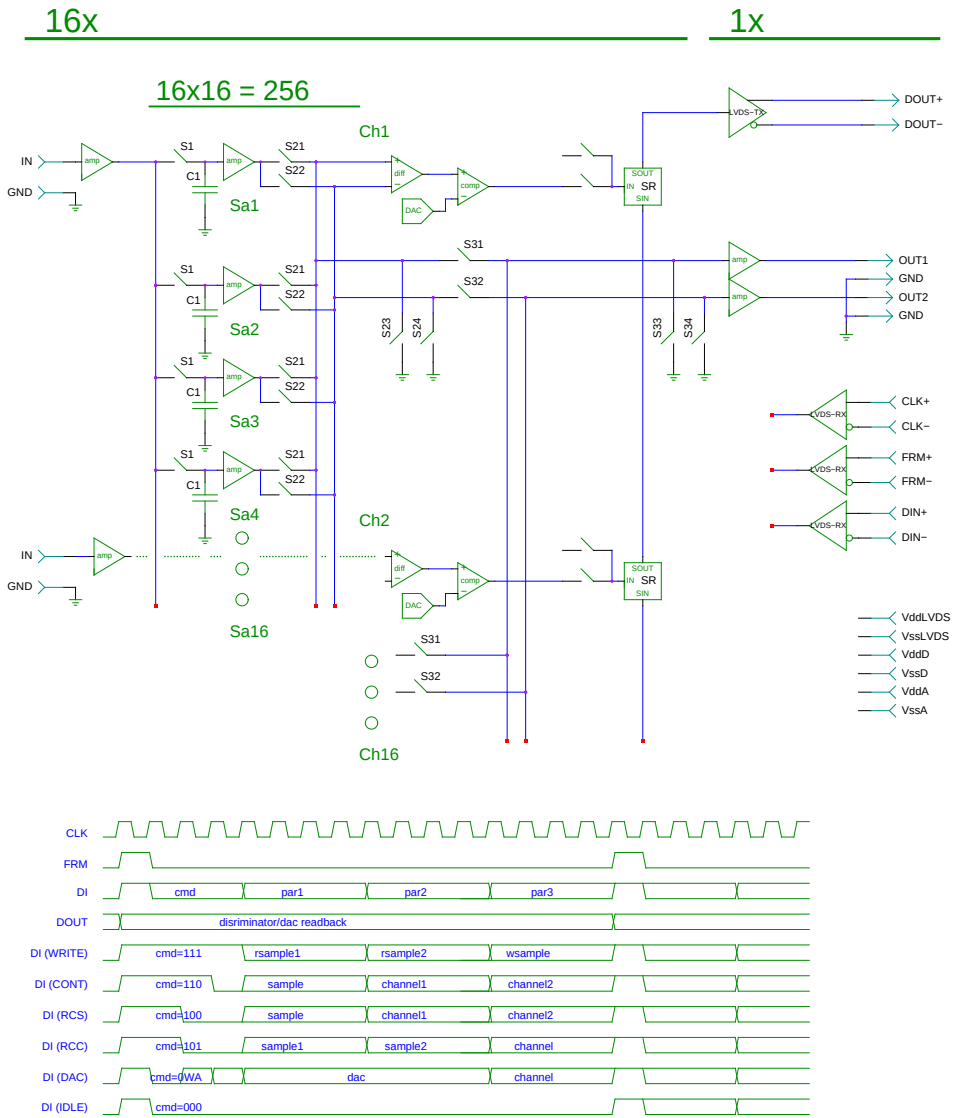
Switched Capacitor Array
16 channels by 16 samples



Specifications:

Size:
- 16 analog input channels, 16 sample capacitors per channel.
- Two independent multiplexed ouputs, that can also be use as a differential pair

Speed:
- CLK frequency 32 MHz.
- 16 CLKs per FRM.
- Analog settling times < 500ns

Digital Interface:
- Three LVDS inputs. (CLK, FRM, DIN)
- One true LVDS driver output. (DOUT)

Resolution:
- 12 bit, i.e., the ratio of signal range to noise amplitude shall be at least 5000, at 32 MHz CLK (2 MSPS).
- Droop rate < 1% full range/ms.

Power: Single analog supply. Independent signal GND. Separate digital and LVDS supplies. All three supplies can be the same voltage, e.g. 3.3V. Power consumption < 10 mW/channel.

Environment:
- Space. TID hardend to 300 krad. Latchup, SEU hardened.

Frame commands:

WRITE:
- S1 selected by wsample
- S21 selected by rsample1
- S22 selected by rsample2
- S3x grounded
- SR discriminator outputs

CONT:
- S1 selected by sample
- S2x selected by sample
- S31 selected by channel1
- S32 selected by channel2
- SR discriminator outputs

RCS: (read common sample)
- S1 open
- S2x selected by sample
- S31 selected by channel1
- S32 selected by channel2
- SR discriminator outputs

RCC: (read common channel)
- S1 open
- S21 selected by sample1
- S22 selected by sample2
- S3x selected by channel
- SR discriminator outputs

DAC:
- WA=10 write the same DAC setting to all channles
- WA=11 write dac setting to channel
- WA=01 do not write, only readback
- SR DAC readback for channel
- S1 open
- S2x grounded
- S3x grounded

IDLE:
- sync internal frame generator ?
- SR zeros
- S1 open
- S2x grounded
- S3x grounded

Intended use:

Sample, in parallel, at 1 to 2 MSPS, sixteen shaper outputs with a continuous stream of write commands to subsequent samples as a circular buffer.

While writing, use the discriminator to compare a recent sample with an early baseline sample. An FPGA serially receives the discriminator results and forms a trigger decision based on coincidences/anticoincidences between the channels. When a positive trigger decision it reached, the trigger also forms a list of channels to read for the particular type of coincidences found.

After a trigger, writing continues for a few more samples to make sure that some samples on the falling edge of the pulse are included, and then stops.

Read frames are then issued for all requested channels. Two ADCs can operate in parallel for speed (RCS), or a baseline sample is selected for output 2 for a differential readout (RCC).

Before resuming write mode, a DAC write/readback shall be issued for good measure, so that after sixteen events all DAC setting were refreshed/verified.

The FPGA does an optimal filtering analysis of the sample stream. AT least five non−continuous samples are required for a good pulse height resolution. The decision which samples to read may depend on the duration/arrival pattern of the discriminator bits on the various channels, but the same set of samples is read for all channels.

The optimal filtering analysis also yields a pulse arival time, or phase of the pulse versus the FRM clock. The phase will be used for a banana correction of the pulse height.

Other use:

The discriminators can be used to operare as an 8−bit successive approximation ADC.

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